**DEPARTMENT OF ELECTRICAL ENGINEERING**

**Course Descriptive File**

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| 1 | Course Title | Digital Logic Design |
| 2 | Course Code | EE 203 |
| 3 | Credit Hours | 4(3,1) |
| 4 | Pre-requisites | Programming Fundamentals |
|  5 |  Co-requisites | Integrated Electronics |
| 6 | Semester | III |
| 7 | Resource Person | Ms. Nausheen Bilal |
| 8 | Contact Hours (Theory) | 3 |
| 9 | Contact Hours (Lab) | 3 |
| 10 | Office Hours  | 8 am to 3 pm |
| 11 | Email | Nausheen192@hotmail.com |
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| 12 | Course Outline as per Scheme of Studies ( SoS) |
| Number Systems, Boolean Algebra, Logic Simplification, Combinational Logic, Sequential Logic, Latches, Flip-Flops and their applications. Adders, Multiplexers, Counters, Shift Registers, and simple Arithmetic Logic Unit (ALU). Design and implementation of combinational circuits in Verilog, Introduction to FPGA.  |
| 13 | Course Objectives as per SoS |
| 1. Understand how logic circuits are used to solve engineering problems.
2. Understand how logic circuits are analyzed, designed, verified and tested.
3. Understand the relationship between abstract logic characterizations and practical electrical implementations.
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| 14 | Books  |
| Textbook1. M. Morris Mano and Micheal D. Ciletti, “Digital Design with an introduction to the Verilog HDL”, Prentice Hall, 5th Edition. 2. Morris Mano and Charles R. Kime, “Logic and Computer Design Fundamentals”, Prentice Hall. Latest Edition Reference Books Tocci and Widmer, "Digital Systems: Principles and Applications". Prentice Hall. Latest Edition  |
| 15 | Course Learning Outcomes (CLOs) |
| After successful completion, students will be able to:Theory CLOs:CLO 1: Transform the decimal numbers to/from binary, octal hexadecimal etc and carry out the simple and signed arithmetic operations in these base systems. CLO 2: Apply K-map and theorem of Boolean algebra to simplify logic equation and use gates and encoders, decoders, multiplexers and de-multiplexers to build circuits. CLO3: Derive equations from truth / state table in order to design synchronous sequential logic which includes latches, flip-flops and state reduction.Lab CLOs:CLO 4: Perform hardware combination of various IC to implement particular functionalities and software simulation on Xilinx ISE platform.  |
| 16 | Marks Breakup  |
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| Quizzes | 10% |
| Homework/assignments  | 10% |
| Midterm exam | 25% |
| Terminal exam (3 hours) | 30% |
| Total (theory) | 75% |

Theory

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| Lab Assessments | 10% |
| Lab Sessional Exams(50% Lab performance + 50% Lab Assessments) | 5% |
| Lab Terminal Exam  (xx% Lab performance + xx% Lab Assessments) | 10% |
| Total (lab) | 25% |

Lab

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| Final marks | Theory marks \* 0.75 + Lab marks \* 0.25 |

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| **17** |
| **Week** | **Topic** | **CLO** | **Taxonomy****Level** | **Specific Outcome** | **Contact Hours** | **Assessment** |
| 1 | Binary numbers, octal and hexadecimal numbers | CLO1  | C1, C2  | After completing these contents the student will be have: 1. Familiarization with binary logic, synthesis and analysis of combinational circuits 2. Introduction to the concept and methods of digital computer arithmetic. 3. Explain concepts and terminology of digital electronics. 4. Represent numbers and perform arithmetic in bases 2, 8, 10, and 16.  | 3+1 | Assignment1 |
| 2 | Number system, Binary logic, Complements | CLO1  | C1  | After completing these contents the student will be have: 1. Clear Concepts used in digital logic design: notation, number systems, difference between analog and digital system, specification and implementation, analysis and design. 2. Familiarization with Boolean (switching) algebra and switching expressions.  | 3+1 | Quiz 1 |
| 3 | Boolean Algebra, Canonical Form | CLO1  | C1, C4 | After completing these contents the student will be able to: 1. Familiarization with logic level models including Boolean Algebra and arithmetic circuits. **2.** Understand Boolean algebra and basic properties of Boolean algebra; able to simplify simple Boolean functions by using the basic Boolean properties.  | 3+1 | Assignment 2  |
| 4 | Boolean functions, Logic operations, Logic gates | CLO1  | C3, C4  | After completing these contents the student will be familiar to: 1. Application of logic to design and creation, using gates, to solutions to a problem. 2. Map the high-level description of a digital system into a binary description of it  | 3+1 | Quiz 2 |
| 5 | Adder Subs tractor, Min Term Max Term | CLO2  | C1, C3, C4 | After completing these contents the student will be able to: **1.** Perform basic arithmetic operations with signed integers  | 3+1 | Assignment 3  |
| 6 | K-Mapping, NAND and NOR Implementation | CLO2  | C2, C4  | After completing these contents the student will be able to: 1. Formulate and employ a Karnaugh Map to reduce Boolean expressions and logic circuits to their simplest forms. 2. Create circuits to solve problems using gates to replicate all logic functions. 3. Design and evaluate a solution to a digital design problem. 4. Analyze and design combinational systems using standard gates and minimization methods  | 3+1 | Quiz 3 |
| 7 | Multilevel NAND and NOR Circuits, Exclusive OR Functions | CLO2  | C2, C3, C4  | After completing these contents the student will be able to: 1. Apply application of logic to design and creation, using gates, to solutions to a problem 2. Create circuits to solve problems using gates to replicate all logic functions 3. Design and evaluate a solution to a digital design problem.  | 3+1 | Assignment 4 |
| 8 | Code Conversion and Analysis Procedure | CLO 2 | C2, C4  | After completing these contents the student will be able to: 1. To apply the principles of Boolean algebra to manipulate and minimize logic expressions. 2. Analyze the concepts of datapaths, control units, and micro-operations and building blocks of digital systems  | 3+1 |  |
| 9 | Magnitude Comparator, Decoders and Encoders | CLO 2   | C1, C2, C4 | After completing these contents the student will be able to: 1. Encode symbols and numbers in binary codes. 2. Add and subtract using 2’s complement code. 3. Evaluate and simplify logical functions using Boolean algebra. 4. Represent logical functions in Canonical form.  | 3+1 | Quiz 4 |
| 10 | PLA, PAL, ROM  | CLO 2  | C1, C4  | After completing these contents the student will be able to: 1. To design combinational circuits using decoders, ROM and transmission gates 2. Perform the operation of state-of-the-art components to design and build complex digital systems, such as memories, PLA, PALs and programmable logic devices (such as FPGAs). 3. Knowledge and use of hardware description languages (VHDL) for system modeling and simulation.  | 3+1 |  |
| 11 | Decoders and Encoders  | CLO 3 | C3, C4  | After completing these contents the student will be able to: 1. Interpret the specifications of programmable reconfigurable devices and select the appropriate device for required application. 2. Design a system, component, or process to meet a set of specifications.  | 3+1 | Assignment 5 |
| 13 | Multiplexers, Flip flops | CLO 3 | C2, C3, C4 | After completing these contents the student will be able to: 1. Familiar with basic sequential logic components: SR Latch, D Flip-Flop and their usage and able to analyze sequential logic circuits. 2. Understand that the design process for today's billion-transistor digital systems becomes a more programming based process than before and programming skills are important. 3. Manipulate and design combination of operators to form higher level functions (multiplexer, counter) and memory element (flip-flop).  | 3+1 | Quiz 5 |
| 14 | Sequential Circuits, State Reduction and Analysis | CLO 3  | C2, C4  | After completing these contents the student will be able to: 1. Introduction to the fundamental principles of sequential circuits. 2. Acquaintance to novel design techniques and implementation technologies of digital systems. 3. Understand the functionality and applications of logic circuits  | 3+1 |  |
| 15 | Memory Decoding, Error Correcting Codes  | CLO 3 | C3, C4  | After completing these contents the student will be able to: 1. Explain different memory structures and technologies. 2. Introduce computational problem-solving technique. 3. Provide Error detection and correction techniques for error free code.  | 3+1 |  |
| 16 | Revision |  |  |  | 3+1 |  |

* Every instructor have his/her plan for course material used for assignments and quizzes, table above is just a guideline.

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| **18** | **Course Learning Outcomes (CLOs) and Assessment Plan** |
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| CLOActivity  | CLO 1 | CLO2 | CLO3 | CLO4 |
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| Quiz 1 | C2, C3 |  |  |  |
| Quiz 2 | C1, C3 |  |  |  |
| Quiz 3 |  | C4 |  |  |
| Assignment 1 | C3, C2 |  |  |  |
| Assignment 2 |  | C4 |  |  |
| Assignment 3 |  | C4 |  |  |
| MID TERM EXAM | C2 | C1, C4 |  |  |
| Quiz 4 |  |  |  |  |
| Quiz 5 |  |  | C1, C2 |  |
| Assignment 4 |  | C1, C4 |  |  |
| Assignment 5 |  |  | C1, C2 |  |
| FINAL TERM EXAM | C1 | C1, C2, C4 | C1, C2 |  |
| Lab Final Exam |  |  |  | C2,C3, C4 |

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| **19** | **Lab Details** |
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| **Laboratory Resources** |
| * IC and trainers
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| **Computer Resources** |
| * Software based (Xilinx ISE)
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| **20** | **Mapping of CLOs to PLOs**  |

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| PLOCLOs | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 |
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| CLO1 |  |  |  |  |  |  |  |  |  |  |  |  |
| CLO2 |  |  |  |  |  |  |  |  |  |  |  |  |
| CLO3 |  |  |  |  |  |  |  |  |  |  |  |  |
| CLO4 |  |  |  |  |  |  |  |  |  |  |  |  |

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| **21** | **List of Experiment With Objectives as Per OBE Format**  |
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| **S. No.** | **Experiment** |
| **1** | Study and Analysis of various types of gates and ICs. |
| **2a** | To check the operation of OR Gate according to OR’s truth table using IC 74LS32. |
| **2b** | To check the operation of NOT Gate according to NOT’s truth table using IC 74LS04. |
| **2c** | To check the operation of AND Gate according to AND’s truth table using IC 74LS08. |
| **3a** | To check the operation of NAND Gate according to NAND’s truth table using IC 74LS00. |
| **3b** | To check the operation of NOR Gate according to NOR’s truth table using IC 74LS02. |
| **3c** | To check the operation of XOR Gate according to XOR’s truth table using IC 74LS86. |
| **4a** | To construct half adder using AND and XOR gate. |
| **4b** | To construct half subtractor using AND, XOR and NOT gate. |
| **5a** | To construct full adder using OR, AND and XOR gate. |
| **5b** | To construct full adder using NAND gate. |
| **6** | To study the operation of Flip flops. |
| **7** | Study the operation of RS using NAND/NOR logics. |
| **8** | Perform gate level and behavioral modeling with verilog simulation of half adder on Xilinx. |
| **9** | Perform gate level and behavioral modeling with verilog simulation of 4 bit ALU on Xilinx. |
| **10** | Perform gate level and behavioral modeling with verilog simulation of half subtractor on Xilinx. |
| **11** | Perform gate level and behavioral modeling with verilog simulation of full subtractor on Xilinx. |
| **12** | Perform gate level and behavioral modeling with verilog simulation of full adder on Xilinx. |

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